

IN THE CLAIMS:

Kindly cancel claims 1-150, without prejudice.

Kindly add the following claims:

Surely 31
151. A controller device for controlling a synchronous dynamic random access
memory device, the controller device comprises:

3 first output driver circuitry to output block size information to the memory device,
4 wherein the block size information defines an amount of data to be output by the
5 memory device; and

6 input receiver circuitry to receive the amount of data output by the memory
7 device.

NOTE 44
152. The controller device of claim 151 further including second output driver
circuitry to output an operation code to the memory device, wherein the operation code
specifies a read operation and, in response to the operation code, the memory device
outputs the amount of data.

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153. The controller device of claim 152 wherein the operation code is included
2 in a packet.

154. The controller device of claim 153 wherein the block size information and
2 the operation code are included in the same packet.

155. The controller device of claim 152 wherein the first output driver circuitry
2 outputs the block size information in response to a first transition of an external clock
3 signal and the second output driver circuitry outputs the operation code in response to a
4 second transition of the external clock signal.

1 156. The controller device of claim 152 wherein the first output driver circuitry
2 and the second output driver circuitry output address information to the memory device.

1 157. The controller device of claim 156 wherein the block size information, the
2 address information and the operation code are output to the memory device via an
3 external bus.

1 158. The controller device of claim 157 wherein the external bus includes a
2 plurality of signal lines to carry, in a multiplexed format, the block size information, the
3 operation code and the address information.

1 159. The controller device of claim 151 further including delay locked loop
2 circuitry, coupled to the input receiver circuitry, to generate an internal clock signal,
3 wherein the input receiver circuitry samples the amount of data in response to the
4 internal clock signal.

1 160. The controller device of claim 151 further including delay locked loop
2 circuitry, coupled to the first output driver circuitry, to generate an internal clock signal,
3 wherein the first output driver circuitry outputs the block size information in response to
4 the internal clock signal.

1 161. The controller device of claim 151 wherein the block size information is a
2 binary code.

1 162. The controller device of claim 151 wherein the input receiver circuitry
2 samples:

3 a first portion of the amount of data during a first half of a clock cycle of the
4 external clock signal; and

5 a second portion of the amount of data during a second half of the clock cycle of
6 the external clock signal.

AN 3
1 163. The controller device of claim 151 wherein the input receiver circuitry
2 samples:

3 a first portion of the amount of data in response to a rising edge of the external
4 clock signal; and

5 a second portion of the amount of data in response to a falling edge of the
6 external clock signal.

TEST 4
1 164. An integrated circuit device comprising:

2 a plurality of output drivers to output block size information to a second integrated
3 circuit device, wherein the block size information represents an amount of data to be
4 output by the second integrated circuit device;

5 a delay locked loop to generate an internal clock signal; and

6 a plurality of input receivers, coupled to the delay locked loop, to sample the
7 amount of data output by the second integrated circuit device, wherein the amount of
8 data is sampled synchronously with respect to the internal clock signal.

1 165. The integrated circuit device of claim 164 further including a clock receiver
2 to receive an external clock signal wherein the delay locked loop generates the internal
3 clock signal using the external clock signal.

1 166. The integrated circuit device of claim 164 wherein the output drivers
2 output the block size information to the second integrated circuit device via a bus,
3 wherein the bus includes a plurality of signal lines.

1 167. The integrated circuit device of claim 166 wherein the plurality of signal
2 lines carry, in a multiplexed format, an operation code, address information and the
3 block size information.

1 168. The integrated circuit device of claim 164 wherein the block size
2 information is a binary code.

1 169. The integrated circuit device of claim 164 wherein the block size
2 information is included in a request packet.

1 170. The integrated circuit device of claim 169 wherein the amount of data
2 output by the second integrated circuit device is included in a data packet.

1 171. The integrated circuit device of claim 170 wherein the data packet is
2 output by the second integrated circuit device onto a set of signal lines, and the request
3 packet is output to the second integrated circuit device via the same set of signal lines.

1 172. The integrated circuit device of claim 164 wherein:

2 during a first half of a clock cycle of the external clock signal, the plurality of input
3 receivers sample a first portion of the amount of data output by the second integrated
4 circuit device; and

5 during a second half of the clock cycle of the external clock signal, the plurality of
6 input receivers sample a second portion of the amount of data output by the second
7 integrated circuit device.

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1 173. The integrated circuit device of claim 164 wherein:

2 the plurality of input receivers sample a first portion of the amount of data output
3 by the second integrated circuit device in response to a rising edge of the external clock
4 signal; and

5 the plurality of input receivers sample a second portion of the amount of data
6 output by the second integrated circuit device in response to a falling edge of the
7 external clock signal.

TO
1 174. An integrated circuit device for controlling a synchronous memory device,
2 the controller integrated circuit comprises:

3 clock receiver circuitry to receive an external clock signal;

4 delay locked loop circuitry, coupled to the clock receiver circuitry, to generate an
5 internal clock signal; and

6 a first plurality of output drivers, coupled to the delay locked loop circuitry, to
7 output an amount of data in response to the internal clock signal.

1 175. The integrated circuit device of claim 174 further including input receivers

2 to sample data that is output by the memory device.

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1 176. The integrated circuit device of claim 175 wherein the input receivers are
2 coupled to the delay locked loop circuitry to sample the data in response to the internal
3 clock signal.

1 177. The integrated circuit device of claim 174 wherein:
2 on a rising edge transition of the external clock signal, the input receivers sample
3 a first portion of the data that is output by the memory device; and
4 on a falling edge transition of the external clock signal, the input receivers sample
5 a second portion of the data that is output by the memory device.

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4 178. The integrated circuit device of claim 174 further including a second
5 plurality of output drivers to output a first operation code to the memory device, wherein
6 the first operation code specifies a read operation, and wherein the memory device, in
7 response to the first operation code, outputs data.

1 179. The integrated circuit device of claim 174 wherein:
2 the first plurality of output drivers output a first portion of the amount of data in
3 response to a rising edge transition of the external clock signal; and
4 the first plurality of output drivers output a second portion of the amount of data in
5 response to a falling edge transition of the external clock signal.

1 180. The integrated circuit device of claim 174 further including a second
2 plurality of output drivers to output a second operation code to the synchronous memory
3 device, wherein the second operation code specifies a write operation, and wherein the
4 memory device, in response to the second operation code, samples the amount of data.

1 181. The integrated circuit device of claim 174 wherein the first plurality of
2 output drivers are coupled to the memory device via an external bus that includes a
3 plurality of signal lines.

1 182. The integrated circuit device of claim 181 wherein the first plurality of output
2 drivers output an operation code and address information to the memory device, in a
3 multiplexed format, via the plurality of signal lines.

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1 183. The integrated circuit device of claim 174 wherein the first plurality of
2 output drivers include a plurality of output drivers to output an operation code to the
3 memory device, wherein the operation code specifies a read operation, and wherein the
4 memory device outputs data in response to the operation code specifying the read
5 operation.

1 184. An integrated circuit controller device for controlling a synchronous
2 dynamic random access memory device, the controller device comprises:

3 a first plurality of output drivers to output block size information to the memory
4 device, wherein the block size information represents an amount of data to be output by
5 the memory device;

6 a second plurality of output drivers to output an operation code to the memory
7 device, wherein the operation code specifies a read operation, and wherein the memory
8 device outputs the amount of data to the controller device in response to the operation
9 code; and

10 a plurality of input receivers to receive the amount of data output by the memory
11 device.

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1 185. The controller device of claim 184 wherein the operation code is included
2 in a packet.

1 186. The controller device of claim 185 wherein the block size information and
2 the operation code are included in the same packet.

1 187. The controller device of claim 184 wherein the block size information is
2 output in response to a first transition of an external clock signal and the operation code
3 is output in response to a second transition of the external clock signal.
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1 188. The controller device of claim 184 wherein both the first plurality of output
2 drivers and the second plurality of output drivers output address information to the
3 memory device.

1 189. The controller device of claim 188 wherein the block size information, the
2 operation code, and the address information are output, in a multiplexed format, to the
3 memory device via an external bus.

1 190. The controller device of claim 184 further including a clock receiver to
2 receive an external clock signal, wherein the first plurality of output drivers outputs the
3 block size information synchronously with respect to the external clock signal.

1 191. The controller device of claim 190 further including a delay locked loop
2 coupled to the clock receiver and the plurality of input receivers, wherein the delay
3 locked loop generates an internal clock signal, and wherein the plurality of input
4 receivers sample the amount of data in response to the internal clock signal.

1 192. The controller device of claim 190 further including a delay locked loop
2 coupled to the first plurality of output drivers and the clock receiver, wherein the delay
3 locked loop generates an internal clock signal, and wherein the first plurality of output
4 drivers circuitry outputs the block size information in response to the internal clock
5 signal.

1 193. The controller device of claim 184 wherein the block size information is a
2 binary code.

1 194. The controller device of claim 184 wherein:
2 the plurality of input receivers samples a first portion of the amount of data during
3 a first half of a clock cycle of the external clock signal; and
4 the plurality of input receivers samples a second portion of the amount of data
5 during a second half of the clock cycle of the external clock signal.

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